REMARKS

Claims 50-57 are pending in the present application. In the Office Action dated April 29, 2005, the Examiner rejected claims 50, 51, 53 and 54 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,237,441 to Nhu ("the Nhu reference") in view of U.S. Patent No. 5,198,684 to Sudo ("the Sudo reference"). Claim 52 was rejected under 35 U.S.C. 103(a) as being unpatentable over the Nhu and Sudo references as applied to claim 1 above, and further in view of U.S. Patent No. 5,200,631 to Austin et al. ("the Austin reference").

The embodiments disclosed in the present application will now be discussed in comparison to the cited references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the cited references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

Figure 3 of the present application shows one embodiment for a microelectronics package 30 having a chip 32 attached to a chip package 34 that communicate with each other without the need for a direct electrical connection. The microelectronic package 30 may be employed in a memory device as described in more detail with respect to Figures 5 and 6. Referring to Figure 3, the chip 32 is attached to a respective chip package 34 and the chip 32 and chip package 34 can transmit information to each other using a set of converters configured for communicating with each other through the emission and reception of electromagnetic signals 42. Both the chip 32 and the chip package 34 have at least one such converter physically disposed on them. The chip 32 includes electronic circuitry 36 coupled to bonding pads 38 which, in turn, are coupled to first converters 40. Each first converter 40 receives a corresponding electric signal 41 from the circuitry 36 via the bonding pad 38, and converts the electric signal into an electromagnetic signal 42. The converter 40 then transmits the electromagnetic signal 42 to a corresponding second converter 44 associated with the chip package 34. The second converter 44 receives the electromagnetic signal 42 and converts it to a corresponding electric signal 45 that is applied to an inner lead 46 of the chip package. The

various converters employed may transmit and receive electromagnetic signals over a wide range of frequencies, including visible light and infrared frequencies.

Accordingly, not having a direct physical electrical connection between the chip 32 and the chip package 34, such as with wire bonding, flip chip bonding, tape automated bonding, etc. decreases the inductive and capacitive effects commonly experienced with such conventional bonding techniques.

The Examiner has cited the Nhu reference for the purposes of disclosing a module having a chip 10 mounted on a chip package 20, and the Applicants acknowledges this teaching therein. However, the Nhu reference does not provide any reason to modify its teachings so that the chip 10 and chip package 20 communicate with each other by the conversion of electromagnetic signals to electric signals. In fact, it clearly teaches away because the chip 10 and the chip package 20 appears to use a conventional direct physical electrical connection therebetween, such as soldering, etc. The Examiner has also cited the Sudo reference in order to provide a purported teaching for modifying the disclosure of the Nhu reference so that the chip 10 and chip package 20 thereof communicate with each other without using a direct electrical connection. Namely, the Sudo reference is used by the Examiner to purportedly provide a teaching to modify the Nhu reference so that the chip 10 and chip package 20 communicate with each other by transmitting electromagnetic signals that are converted by a converter to an electric signal.

The Sudo reference is directed to solving the problem of reducing signal distortion between a plurality of semiconductor modules (referred to as "semiconductor packaging substrates 10" in the Sudo reference). This problem is clearly stated when the Sudo reference states that "an object of the present invention is to provide a high-performance semiconductor integrated circuit device wherein distortion of a signal waveform, which may occur in a signal transmission path between semiconductor packaging substrates [semiconductor modules], is prevented and the delay time is decreased." (Col. 2, lines 21-27). To achieve this object of reducing the delay time between semiconductor modules, the Sudo reference optically communicates between adjacent semiconductor modules. (Col. 2, lines 28-53). The Sudo reference is not concerned with how a chip and chip package of a given semiconductor module communicate with each other. As shown in Figures 1 and 2, the semiconductor module 10

includes a silicon substrate 20 and semiconductor chips 30 flip chip mounted thereto on the silicon substrate 20. The semiconductor chips 30 include solder bumps 65 that are electrically connected to the silicon substrate 20. Each module 10 also includes a light transmit-receive elements 40A and 40B disposed at openings 50 provided on both sides of the center portion of the silicon substrate 20. The elements 40A and 40B respectively comprise photodiode chips 42A and 42B, and semiconductor laser chips 44A and 44B. As shown in Figures 1 and 2, a plurality of modules 10 may be spaced apart and stacked together so that light transmit-receive elements 40A and 40B may optically communicate with each other.

Therefore, the Sudo reference teaches that respective modules 10 optically communicate with each other in order to solve the delay time problem between modules 10. There is no teaching or suggestion that the semiconductor chip 30 and its underlying silicon substrate 20 in a given module 10 should optically communicate with each other. In fact, the Sudo reference does not teach that there is any problem with conventional electrical connections between the semiconductor chip 30 and the silicon substrate 20. The way that the communication is effected between the semiconductor chip 30 and the silicon substrate 20 does not appear to be relevant to solving the delay time problem between adjacent modules 10.

The combination of the teachings of the Nhu and Sudo references teach an electrical device assembly that is very different than that purported by the Examiner. The modification of the Nhu reference with the Sudo reference results in a module having the chip 10 mounted on the chip package 20 in optical communication with another identical module having another chip 10 mounted on another chip package 20. By providing optical communication between modules, any delay time problem can be solved. There is simply no teaching, either express or implied, in the Nhu and Sudo references for optical communication between a chip attached to a chip package of the same module.

Applicants understand that motivation to modify a reference does not need to be expressly articulated by the cited references, although if there is motivation to combine or modify a reference such motivation is usually expressly found in the references. However, the Examiner still must articulate a credible motivation to modify the cited references, either from the express or implied teachings of the cited references or from knowledge commonly known to those of ordinary skill in the art. A reason has not been articulated why one of ordinary skill in

the art would modify a conventional memory device as in the Nhu reference so that the chip 10 communicates with the chip package 20 using, for example, optical communication as in the Sudo reference. The portion of the background of the Nhu reference cited by the Examiner for motivation refers to being able to better integrate computer peripherals with the module that comprises the chip 10 and chip package 20. The invention of the Nhu reference achieves this object by using the optical fiber connectors 22. Again, a teaching to provide greater computer peripheral integration does not provide a teaching to modify the manner in which the chip 10 and the chip package 20 of the Nhu reference communicate with each other.

In summary, the combination of the Sudo and Nhu references do not teach modifying a conventional chip-on-chip package as disclosed in the Nhu reference so that the chip attached to the chip package communicate with each other using a set of converters that are operable to convert electromagnetic signals to electric signals.

Turning now to the claims, the patentably distinct differences between the cited references and the claim language will be specifically pointed out. Claim 50 recites, in part, "a chip package attached to the chip, the chip package including a second converter that is operable to receive the data output electromagnetic waves from the first converter and convert these received electromagnetic waves into corresponding electric data output signals that are applied to corresponding conductors, and the second converter operable to receive electric address, data, and control signals on corresponding conductors and to convert these electric signals into corresponding address, data, and control electromagnetic waves that are communicated to the first converter." The cited references do not teach or suggest a chip package attached to the chip, wherein the chip and chip package communicate with each other by the conversion of electromagnetic signals to electric signals or vice versa. Furthermore, there is no motivation or suggestion to combine the Nhu reference and the Sudo reference to achieve the present invention of claim 50. Any combination of the Nhu reference and the Sudo reference would result in employing the light transmit-receive elements 40A and 40B of the Sudo reference to enable optical communication between a plurality of the modules of the Nhu reference which are comprised of a chip package 20 having a chip 10 attached and conventionally electrically connected thereto.

Claims depending from claim 50 are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims. For example, as required by claim 56, none of the cited references discloses or fairly suggest the chip having the first converter mounted on a first side and the chip package having the second converter mounted on a first side thereof, the first side of the chip being adjacent to the first side of the chip package. Again, as required by claim 57, none of the cited references discloses or fairly suggests the chip having a first side and a second side opposing the first side, the first converter being mounted on the first side, and the chip package including a first side on which the second converter is positioned, the chip being attached to the chip package with the second side of the chip positioned adjacent the first side of the chip package

All of the claims remaining in the application (claims 50-57) are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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